REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 1-13 were pending in this case. Non-elected Claims 1-4 have been cancelled without prejudice. New Claims 14-19 have been added. Claims 5-9 and 12 have been amended to correct grammar and informalities.

In the Drawings, Figure 10 was objected to. A proposed correction in which Figure 10 is labelled "Prior Art" is attached hereto.

The disclosure was objected to for informalities on Page 12. The specification has been amended in response to the objection.

The abstract was objected to as being in an improper format. The abstract has been amended in response to the objection.

Applicant thanks the Examiner for indicating the allowability of Claims 11 and 13. As indicated below, Applicant believes that all of the claims are patentable over the cited art, so Applicant respectfully declines to rewrite Claims 11 and 13 in independent form at this time.

Claims 5, 6, 7, and 9 were objected to for informalities. The Claims have been amended in response to the objection.

Claims 5 and 6 stand rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art. Applicant respectfully traverses the rejection. Claim 5, as amended, includes the step of "forming a two-dimensional plurality of through holes in said insulation film at a pitch *p* between the rows of

sprocket holes." Applicant's admitted prior art, including Figure 10, does not disclose such a feature. Applicant's admission on Page 1, line 29, is that "[b]eneath the region of this circuit pattern 114, multiple through holes are formed prior to formation of this circuit (not shown in the figure)." This in no way implies a two-dimensional plurality of through holes at a pitch *p*. Therefore, Applicant respectfully requests that this rejection be withdrawn. Claim 6 depends from Claim 5 and is therefore patentable for at least the reasons presented above. In addition, Applicant disagrees with the Examiner's statement that "a plurality of through holes . . . must have a pitch *p*," which seems to imply that any plurality of holes must be regularly spaced. Since Applicant's admissions certainly do not say or imply so, Applicant respectfully requests that the Examiner cite prior art references to support this assertion.

Applicant also disagrees with the assertion that the terms *n*, *m*, *L* or *p* are not defined in the specification. See, for example, Applicant's Figure 2 as well as the second paragraph on page 7 of the specification. Moreover, the *L*, *m*, and *n* values are explicitly stated for the embodiment described in the specification, and the *p* value can be easily deduced since *L* is stated to be 4.75 mm, *n* is equal to 2, and *m* is equal to 19. $p = n\,L/m = 0.5$ mm. The variables are thus defined and shown in use in an example. Therefore, Applicant respectfully requests that the rejection be withdrawn.

Claims 7, 8, and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Cho (U.S. Patent No. 6,235,555). Applicant respectfully traverses the rejection. Claims 7, 8, and 12 depend directly or indirectly from Claim 5. Claim 5, as amended, includes the step of "forming a two-dimensional plurality of through holes in said insulation film at a pitch *p* between the rows of sprocket holes." As indicated above, Applicant's admitted prior art does not teach or suggest such a step. Cho does not cure this deficiency. Indeed, in Cho's Figure 10A, it is clear that via holes 62 are not arranged in a two-dimensional plurality at a given pitch (the vertical spacing of the holes, relative to the page, is greater than the horizontal spacing). Since

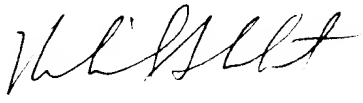
neither Applicant's admissions nor the cited reference teach or suggest the claimed features, Applicant submits that Claim 5 is patentable over the combination. Claims 6, 7, 8, and 12 depend from Claim 5 and are therefore patentable over the combination for at least the reasons presented above.

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art. Applicant respectfully traverses the rejection. Claim 9, as amended, includes the step of "forming a two-dimensional plurality of through holes at a pitch *p* between the rows of sprocket holes." As indicated above with respect to Claim 5, Applicant's admitted art does not teach or suggest such a feature. Therefore, Applicant requests that the rejection be withdrawn.

New Claim 14 includes the step of "providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional plurality of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another at a pitch *p*." The references of record do not show or suggest such a feature. Claims 15-19 depend from Claim 14. Applicant respectfully request that these claims in addition to Claims 5-13 be passed to issuance.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 5-19. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicants' attorney at the below listed telephone number and address.

Respectfully submitted,



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Version with Markings to Show Changes Made

In the Specification:

On page 11, in the fourth paragraph,

-- During step 803 and FIG. 9(C), resin sealing of each semiconductor chip 90 is carried out by means of a mold 94. This molding step uses a mold having cavities (i.e. three cavities) corresponding to the regions of blocks 24A through 24C (refer to FIG. 4 and FIG. 6) demarcated by main line 20. Molding compound fed to the mold flows through runners (each cavity in this working example is provided with two runners) into each cavity, and multiple semiconductor chips 90 placed within these blocks are covered simultaneously. The region upon insulation film 10 covered by mold 94 includes the above mentioned sub-line 22 of the conductor pattern. Moreover, the above mentioned main line 20 of conductor pattern 18 [20] may be partially or entirely included.—

On page 12, in the third paragraph,

-- As described above, multiple semiconductor packages 102 are produced simultaneously using the above mentioned insulation film 10. During the above mentioned manufacturing , most of the region enclosed by main line 20 of the conductor pattern upon insulation film 10 (with the exceptions of the region of sub-line 22 removed by dicing and the region adjacent to main line 20) is used as a region of the substrate of the semiconductor package. The region of discarded insulation film becomes [become] extremely small.—

In the Abstract:

-- [The problem of the present invention is to provide an insulation film capable of highly universal use for the production of semiconductor packages of different sizes and shapes.

The present invention relates to an] An insulation film for providing an insulation substrate carrying a semiconductor chip of a semiconductor package. Insulation film 10 [of the present invention] is provided with rows of opposing sprocket holes 12 formed on either edge of the above mentioned insulation film, and through holes 14 are [provided] disposed two-dimensionally between the rows of sprocket holes 12. Pitch p between through holes 14 is determined by the relationship $m\,p = n\,L$ (i.e., n and m are integers, and $n<m$), wherein pitch of the sprocket holes is taken to be L. [The above mentioned through] Through holes 14 are selectively utilized during formation of the desired circuit pattern upon insulation film 10 according to size of the manufactured semiconductor package.

[[Selected Figure] FIG. 1]--

In the Claims:

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (amended) A method for manufacture of an insulation film for providing an insulation substrate for carrying a semiconductor chip of a semiconductor package comprising the steps of:

providing an insulation film having two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film; and

forming a two-dimensional plurality of through holes in said insulation film [two-dimensionally] at a pitch *p* between the rows of sprocket holes.

6. (amended) The method for manufacture of an insulation film according to claim 5 wherein the pitch *L* and the pitch *p* satisfy the following equation: $m\,p = n\,L$ wherein *n* and *m* are integers that satisfy the equation $n < m$.

7. (amended) The method for manufacture of an insulation film according to claim 6 wherein the step of forming the through holes further comprises the steps of:

forming the through holes by collective punching out at the effective sprocket hole formation width of the through holes along the transverse direction of the insulation film in a region of length $n\,L$ along the length-wise direction of the insulation film;

moving the insulation film a length *n L* in the length-wise direction by means of the sprocket holes; and

repeating these two steps alternately.

8. (amended) The method for manufacture of an insulation film according to claim 6 wherein the method further comprises a step of forming a two-dimensional plurality of circuit patterns [two-dimensionally] upon the insulation film according to size of the semiconductor package and a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

9. (amended) A method for manufacture of a semiconductor package comprising the steps of: providing an insulation film, forming two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film, forming a two-dimensional plurality of through holes [two-dimensionally] at a pitch *p* between the rows of sprocket holes, forming a two-dimensional plurality of circuit patterns [two-dimensionally] upon the insulation film according to size of the semiconductor package, forming a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip with the circuit pattern;

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film.

10. The method for manufacture of a semiconductor package according to claim 9 wherein the method further comprises the step of plating each of the circuit patterns upon the insulation film using the for-plating-electricity-supply-use conductor pattern.

11. The method for manufacture of a semiconductor package according to claim 9 wherein the dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern whereby the sub-line is not left behind upon the insulation film.

12. (amended) The method for manufacture of an insulation film according to claim 7 wherein the method further comprises a step of forming a <u>two-dimensional</u> plurality of circuit patterns [two-dimensionally] upon the insulation film according to size of the semiconductor package and a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

13. The method for manufacture of a semiconductor package according to claim 10 wherein the dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern whereby the sub-line is not left behind upon the insulation film.

Please add the following new claims:

--14. (new) A method of packaging a semiconductor device, comprising the steps of:

providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional plurality of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another at a pitch *p*;

mounting a semiconductor chip over a number of said through holes;

sealing said semiconductor chip and a portion of said insulation film in resin; and

cutting said insulation film surrounding said semiconductor chip to release said resin-sealed chip from the remainder of said insulation film.

15. (new) The method of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional plurality of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another at a pitch *p* and continuously along and transversely across said film within circuit pattern regions on said film.

16. (new) The method of Claim 15, wherein said circuit pattern regions are separated by sub-lines of a conductor pattern, and wherein said step of cutting said insulation film comprises cutting said film with a blade having a blade trim width wider than said sub-line whereby said sub-line is not left behind upon the insulation film after said cutting step.

17. (new) The method of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional plurality of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another at a pitch *p* and continuously along and transversely across said film.

18. (new) The method of Claim 14, further comprising the step of depositing solder in selected ones of said number of through holes.

19. (new) The method of Claim 14, further comprising the step of depositing metal in selected ones of said number of through holes.--